SEMICONDUCTOR PACKAGE, METHOD OF PRODUCTION OF SAME, AND SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

A semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, wherein a topmost stacked structure of the multilayer interconnect structure includes a capacitor structure, the capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of high dielectric constant inorganic filler and insulating resin and including chip connection pads for directly connecting top electrodes and bottom electrodes with electrodes of the semiconductor chip, whereby greater freedom in design of interconnect patterns can be secured, the degree of proximity of the capacitor and semiconductor chip can be greatly improved, and the package can be made smaller and lighter in weight, a method of production of the same, and a semiconductor device using this semiconductor package.